Chapter #7: Sequential Logic Case Studies

7.6 Random Access Memories
Random Access Memories

Transistor efficient methods for implementing storage elements

Small RAM: 256 words by 4-bit

Large RAM: 4 million words by 1-bit

We will discuss a 1024 x 4 organization

Static RAM

The circuit configuration holds a 1 or 0 as long as the system continues to receive power

Static Rams are the fastest memories and the easiest to interface with.
Random Access Memories

Basic storage element of the SRAM is a 6-transistor circuit.

Words = Rows

Static RAM Cell

Columns = Bits (Double Rail Encoded)

Nmos transistors provide access to the storage element from two buses, denoted Data\textsubscript{j} and Data\textsubscript{j}'.

To write the memory element, special circuitry in the RAM drives the data bit and its complement onto these lines while the word enable line is asserted.

To read the contents of the storage element, the word enable line is asserted. The data are sensed by a different collection of special circuits. These circuits detect small voltage differences between the data line and its complement.
Random Access Memories

Static RAM Organization

Chip Select Line (active low)

Write Enable Line (active low)

10 Address Lines to yield 1024 words

4 Bidirectional Data Lines
(used for reading and writing data)

WE determines direction:
‘0’ -- write
‘1’ -- read
Random Access Memories

**RAM Organization**

Long thin layouts are not the best organization for a RAM

- Some Addr bits select row
- Some Addr bits select within row

![Diagram of RAM organization with labeled components: Address Buffers, Row Decoders, Storage Matrix, Sense Amplifiers, Data Buffers, I/O0, I/O1, I/O2, I/O3, CS, WE, and Amplifiers & Mux/Demux.](image)
Random Access Memories

RAM Timing

Simplified Read Timing

Memory access time -- time it takes for new data to be ready to appear at the output
Random Access Memories

RAM Timing

Simplified Write Timing

Memory cycle time -- time between subsequent memory operations.
Random Access Memories

*Dynamic RAMs -- densest memories*

- High capacity due to efficient memory element:
  - 1 Transistor (+ capacitor) memory element
  - Read: Assert Word Line, Sense Bit Line
  - Write: Drive Bit Line, Assert Word Line (charge capacitor with the desired logic voltage)
  - Destructive Read-Out (to read contents of storage capacitor, must discharge it across the bit line)
- Need for Refresh Cycles: storage decay in ms
- Internal circuits read word and write back
Random Access Memories

**DRAM Organization**

Long rows to simplify refresh

Two new signals: RAS, CAS
- Row Address Strobe
- Column Address Strobe

replace Chip Select

- Row Address Decoders
- Storage Matrix 64 x 64
- Column Address & Control Signals
- Column Latches, Multiplexers/Demultiplexers
- Control Logic
- A11
- A0
- RAS
- CAS
- WE
- DIN
- DOUT

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**Random Access Memory**

**RAS, CAS Addressing**

Even to read 1 bit, an entire 64-bit row is read!

Separate addressing into two cycles: Row Address, Column Address
Saves on package pins, speeds RAM access for sequential bits!

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**Address**

- **Row Address**
- **Col Address**

**Read Cycle**

- **RAS**
- **CAS**

**Dout**

- **Valid**

**Read Row**

- **Row Address Latched**

**Read Bit Within Row**

- **Column Address Latched**

**Tri-state Outputs**
Random Access Memory

Write Cycle Timing

(1) Latch Row Address
Read Row

(2) WE low

(3) CAS low: replace data bit

(4) RAS high: write back the modified row

(5) CAS high to complete the memory cycle
Random Access Memory

RAM Refresh

Refresh Frequency:

4096 word RAM -- refresh each word once every 4 ms
Assume 120ns memory access cycle
This is one refresh cycle every 976 ns (1 in 8 DRAM accesses)!
But RAM is really organized into 64 rows
This is one refresh cycle every 62.5 µs (1 in 500 DRAM accesses)
Large capacity DRAMs have 256 rows, refresh once every 16 µs

RAS-only Refresh (RAS cycling, no CAS cycling)
External controller remembers last refreshed row

Some memory chips maintain refresh row pointer
CAS before RAS refresh: if CAS goes low before RAS, then refresh
Random Access Memory

DRAM Variations

Page Mode DRAM:
read/write bit within last accessed row without RAS cycle
RAS, CAS, CAS, . . ., CAS, RAS, CAS, ...
New column address for each CAS cycle

Static Column DRAM:
like page mode, except address bit changes signal new cycles rather than CAS cycling
on writes, deselect chip or CAS while address lines are changing

Nibble Mode DRAM:
like page mode, except that CAS cycling implies next column address in sequence -- no need to specify column address after first CAS

Works for 4 bits at a time (hence "nibble")
RAS, CAS, CAS, CAS, CAS, RAS, CAS, CAS, CAS, CAS, CAS, CAS, . . .